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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,551	Applicant(s) Lian Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov 10, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 2, 4-8, 10-13, 21-29, 32, and 33* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 4-8, 10-13, 21-29, 32, and 33* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a request for reconsideration filed November 10, 2003.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7, 8, 13 and 21-27 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278) in view of Marsch et.al. (U.S. Patent No. 6,617,634).

With regard to Claim 1, Nakabayashi teaches a conductive barrier layer (column 10, lines 38-49) and an electrode (25) comprising a first conductive liner (Ir) disposed over and electrically coupled to the conductive barrier layer, a second conductive liner (IrO_2) disposed over the first conductive liner, the second conductive liner being electrically coupled to the first conductive liner and the conductive barrier layer and a conductive layer (Ir) disposed over the second conductive liner, the conductive layer being electrically coupled to the first conductive liner, the conductive barrier layer and the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material, see figure 8H.

However, Nakabayashi fails to teach that the second conductive liner has a thickness from about 20 to about 50 angstroms. Marsch discloses an integrated circuit device including an conductive layer (24) comprising iridium oxide (column 5, lines 30-40) having a thickness of about 50 angstroms (column 5, line 25). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a second conductive liner having a thickness from about 20 to about 50 angstroms, as suggested by Marsch, in order to provide a conductive layer with a thickness suitable for a capacitor structure (column 5, lines 26-29).

With regard to Claim 2, Nakabayashi teaches a second conductive liner (IrO_2) of the lower electrode (25) comprising a conductive oxide.

With regard to claims 5 and 11, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include the thickness of the first and second conductive liners as claimed, in order to reduce oxygen diffusion into a conductive layer such as polysilicon below the multi-layer electrode.

With regard to Claim 7, Nakabayashi teaches an integrated circuit comprising a FRAM (column 9, lines 48-49).

With regard to Claim 8, Nakabayashi teaches a conductive barrier layer (column 10, lines 38-49) and an electrode (25) comprising a first conductive liner (Ir) deposited over and abutting the conductive barrier layer, the first conductive liner comprising a molecular grain structure having a plurality of columns, a second conductive liner (IrO_2) deposited over and abutting the first conductive liner, the second conductive liner comprising a conductive oxide and a conductive layer (Ir) disposed over and abutting the second conductive liner, the conductive layer comprising a molecular grain structure having a plurality of columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, this is because of the presence of the conductive oxide between first conductive liner and the conductive layer, see figure 8H.

However, Nakabayashi fails to teach that the second conductive liner has a thickness from about 20 to about 50 angstroms. Marsch discloses an integrated circuit device including a conductive layer (24) comprising iridium oxide (column 5, lines 30-40) having a thickness of about 50 angstroms (column 5, line 25). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a second conductive liner having a thickness from about 20 to about 50 angstroms, as suggested by Marsch, in order to provide a conductive layer with a thickness suitable for a capacitor structure (column 5, lines 26-29).

With regard to Claim 13, Nakabayashi teaches an integrated circuit comprising a FRAM (column 9, lines 48-49).

With regard to Claims 21 and 22, Nakabayashi teaches a second conductive liner comprising IrO_2.

With regard to Claims 23 and 24, Nakabayashi teaches a conductive layer and a first conductive liner comprising Ir.

With regard to Claims 25 and 27, Nakabayashi teaches a second conductive liner (IrO_2) comprises a thickness such that the second conductive liner is etchable by the same etchant used to etch the first conductive liner (Ir) and the conductive layer (Ir).

With regard to Claim 26, Nakabayashi teaches an electrode (25) having a conductive layer (Ir) comprising a molecular grain structure having columns, the conductive layer including a top surface, wherein the first conductive liner (Ir) comprises a molecular grain structure having columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, this is because of the presence of the conductive oxide (IrO_2) between first conductive liner and the conductive layer.

Claims 4, 10, 28, 29, 32 and 33 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278) in view of in view of Marsch et.al. (U.S. Patent No. 6,617,634) and further in view of Ramesh (U.S. Patent No. 5,838, 035). With regard to Claims 4 10 and 33, Nakabayashi and Marsch essentially discloses the claimed invention but fail to show, that the conductive layer and the first conductive liner comprise platinum. Ramesh discloses a capacitor stack with a multi-layer electrode including a barrier layer (72) over a conductive plug (42) of polysilicon, a first conductive layer (74) comprising platinum and a second conductive layer (78) also comprising platinum, see figure 4. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi and Marsch to include a conductive layer and a first conductive liner wherein both comprise platinum, as clearly suggested by Ramesh, in order to provide an electrode structure which makes use of conductive layers with materials from the precious metals group, which includes platinum, known for its conductivity in ferroelectric capacitors (column 5, lines 12-13).

With regard to Claim 28, Nakabayashi teaches a conductive barrier layer (column 10, lines 38-49) and an electrode (25) comprising a first conductive liner (Ir) disposed over and electrically coupled to the conductive barrier layer, a second conductive liner (IrO_2) disposed over the first conductive liner, the second conductive liner being electrically coupled to the first conductive liner and the conductive barrier layer and a conductive layer (Ir) disposed over the second

conductive liner, the conductive layer being electrically coupled to the first conductive liner, the conductive barrier layer and the second conductive liner, wherein the conductive layer and the first conductive liner comprise the same material, see figure 8H.

However, Nakabayashi fails to teach that the second conductive liner has a thickness from about 20 to about 50 angstroms. Marsch discloses an integrated circuit device including an conductive layer (24) comprising iridium oxide (column 5, lines 30-40) having a thickness of about 50 angstroms (column 5, line 25). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a second conductive liner having a thickness from about 20 to about 50 angstroms, as suggested by Marsch, in order to provide a conductive layer with a thickness suitable for a capacitor structure (column 5, lines 26-29).

Nakabayashi also fails to show, that the conductive layer and the first conductive liner comprise platinum. Ramesh discloses a capacitor stack with a multi-layer electrode including a barrier layer (72) over a conductive plug (42) of polysilicon, a first conductive layer (74) comprising platinum and a second conductive layer (78) also comprising platinum, see figure 4. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Nakabayashi to include a conductive layer and a first conductive liner wherein both comprise platinum, as clearly suggested by Ramesh, in order

to provide an electrode structure which makes use of conductive layers with materials from the precious metals group, which includes platinum, known for its conductivity in ferroelectric capacitors (column 5, lines 12-13).

With regard to Claim 29, Nakabayashi teaches a second conductive liner comprising IrO_2.

With regard to Claim 32, Nakabayashi teaches an electrode (25) having a conductive layer (Ir) comprising a molecular grain structure having columns, the conductive layer including a top surface, wherein the first conductive liner (Ir) comprises a molecular grain structure having columns, wherein the columns of the conductive layer are not aligned with the columns of the first conductive liner, this is because of the presence of the conductive oxide (IrO_2) between first conductive liner and the conductive layer.

Claims 6 and 12 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nakabayashi (U.S. Patent No. 5,905,278) in view of in view of Marsch et.al. (U.S. Patent No. 6,617,634) and further in view of Yokoyama et.al. (U.S. Patent No. 6,313,539). With regard to Claims 6 and 12, Nakabayashi and Marsch essentially disclose the claimed invention but fail to show, a barrier layer comprising TaSiN. Yokoyama discloses a semiconductor memory device including a barrier layer (516) comprising TaSiN, see figure 22C. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the

structure as taught by Nakabayashiand Marsch to include a barrier layer comprising TaSiN, as clearly suggested by Yokoyama, in order to provide barrier layer comprising a material known for its anti-heat and anti-oxidation properties (column 13, lines 29-32).

Response to Arguments

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. Claim 33 has been treated accordingly and it is reflected in this office action.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached through a direct telephone call, you might call Supervisor Tom Thomas at (703) 308-2772. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

11/26/03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER